REMARKS

No amendments, cancellations, or additions have been made to the present claims. Claims 1-5 and 11-20 remain pending in the case. Further examination and reconsideration of the presently claimed application is respectfully requested.

Section 102 Rejections

Claims 1, 3-5, and 11-20 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,530,057 to Kimmitt (hereinafter "Kimmitt"). The standard for "anticipation" is one of fairly strict identity. A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. Of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987), MPEP 2131. More specifically, "all words in a claim must be considered when judging the patentability of that claim against the prior art." *In re Wilson* 424 F.2d. 1382 (CCPA 1970). Kimmitt does not disclose all limitations of the currently pending claims, some distinctive limitations of which are set forth in more detail below.

Kimmitt fails to anticipate a method for performing a cyclic redundancy check (CRC) calculation on a data stream, where the method includes: (i) determining which one of a plurality of CRC modules -- each configured to perform the CRC calculation on a different number of bytes of data -- should be used for processing a segment of data currently supplied to the multiple-byte CRC circuit, and (ii) after said step of determining, processing the segment of data using only the CRC module determined appropriate for the current segment of data. Independent claim 1 recites, in part:

> A method of performing a cyclic redundancy check (CRC) calculation on a data stream composed of one or more segments of data, the method comprising: supplying the data stream, one data segment per cycle, to a multiple-byte cyclic redundancy check (CRC) circuit comprising a plurality of CRC modules, wherein each of the CRC modules is configured to perform the CRC calculation on a different number of bytes of data during a single cycle; determining which one of the plurality of CRC modules should be used for processing a segment of data currently supplied to the multiple-byte CRC circuit; after said step of determining, processing the segment of data using only the CRC module determined appropriate for the current segment of data, wherein said step of processing comprises performing the CRC calculation on the current segment of data to produce CRC calculation results for the current cycle ...

The present specification discloses that each of a plurality of CRC modules may be configured to perform a CRC calculation on a different number of bytes of data during a single cycle. After determining which CRC module should be used for processing a segment of data, the presently claimed method processes the segment of data using only the selected CRC module. *See*, e.g., Specification, pages 10-11 and 15-18. These features are simply not disclosed by Kimmitt.

However, statements in the final Office Action suggest that Kimmitt provides teaching for all limitations of present claim 1, and more specifically, that teaching for the present limitations may be found in columns 14-15 and Fig. 7 of Kimmitt (*See*, final Office Action, pages 3-4). The Applicant respectfully disagrees. As set forth in more detail below, Kimmitt simply fails to anticipate all limitations of present claim 1. As such, Applicants contend that the § 102 rejection of present claim 1, and all claims dependent therefrom, cannot be maintained.

In columns 14-15, Kimmitt discloses a 32-bit wide CRC generator-checker including "CRC logic modules 100, remainder registers 102, input data register 104, CRC Controller State Machine 106, multiplexer 108, and inverter [110]." (Kimmitt, column 14, lines 35-43; Fig. 7). Kimmitt further teaches that, during operation of the embodiment shown in Fig. 7, "input data 50 is received into the input register 104, and subsequently input to the CRC logic modules 100. The input data is passed to the CRC logic modules 100 in 32 bit portions ... [t]he outputs of the CRC modules 100 are then stored in the remainder registers 102, and fed back as r31 ... r0 135 into the CRC logic modules 100. This process repeats recursively until all the input data 50 has been processed." (Kimmitt, column 14, lines 45-54).

As such, Kimmitt discloses a method in which an input data stream (50) is supplied to a CRC circuit having a plurality of CRC modules (100a-100d), each configured for processing 32 bits of data (r31 ... r0) at a time. In the method disclosed by Kimmitt, each one of the CRC modules processes 32 bits of data, and outputs a CRC result to a corresponding 32 bit remainder register (102a-102d). Kimmitt further teaches that, "[a]t the end of the input data 50, the multiplexer 108 outputs the final contents of a selected one of the 32-bit remainder registers 102, based on the assertion of its controls 112." (Kimmitt, column 14, lines 54-59).

As pointed out by the Examiner, Kimmitt also proposes a method for handling termination sequences (i.e., the last data segment in a data stream) with less than 32 valid bits. For example, Kimmitt discloses that, "logic blocks 100a, 100b and 100c are termination logic blocks for handling termination sequences having 24, 16 and 8 valid bits respectively." (Kimmitt, column 15, lines 18-20; Fig. 7).

Kimmitt also discloses that, when the last word of a message is detected (e.g., by assertion of last word signal 109), CRC controller state machine 106 "detects the number of valid bytes in the last word from valid bytes signal 107. The CRC controller state machine 106 also appends n zero bits at the end of the message... by selecting the hardwired zero input 111 of the multiplexer 104 when the final byte of the last word of the message has been received. The CRC controller state machine 106 then selects which remainder register of remainder registers 102 holds the last value to be passed through the multiplexer 108." (Kimmitt, column 15, lines 24-32). As such, the method of Kimmitt appears to handle termination sequences by padding the last word of the message with zeros (if the number of valid bytes in the last word is less than the standard 32 bits), supplying the (zero padded) last word to CRC modules 100a-100d, and selecting the appropriate CRC result from one of the remainder registers 102a-102d, depending on the number of valid bytes in the last word.

On page 3 of the final Office Action, the Examiner alleges that CRC controller state machine 106 is used "for determining which one of the CRC modules 100a to 100d should be used for processing the segment of data currently supplied to the Multi-byte CRC circuit." More specifically, the Examiner suggests that "CRC Controller State Machine 106 processes data in 4-byte data segments until the last segment of data is reached whereby CRC Controller State Machine 106 uses the size of the last segment to determine which CRC module will be used" (Final Office Action, page 3). However, contrary to the presently claimed case, the CRC controller state machine of Kimmitt does not determine which CRC module (100a-100d) to use before the last word is processed, and instead, processes the last word using all CRC modules. As such, CRC controller state machine 106 fails to select only one CRC module for processing the final bits of the last word.

For example, Kimmitt discloses that the CRC controller state machine (106) supplies a 32 bit data segment to all CRC modules (100a-110d) by padding the valid bits in the last word with zeros, if necessary (e.g., if the last word is less than 32 bits in length). *See*, e.g., Kimmitt, column 15, lines 6-32. After all CRC modules (100a-110d) have been used to calculate a CRC result from the (zero padded) 32 bits of the last word, CRC controller state machine 106 selects the appropriate CRC result from one of the remainder registers (102a-102d), where selection is based on the number of valid bits in the last word. For example, Kimmitt states, "if there are 8 valid bits in the final word, the CRC controller state machine operates to select the remainder register 102a using the controls 112 of the multiplexer 108, if there are 16 valid bits, the contents of remainder register 102b is selected," etc. (Kimmitt, column 15, lines 35-41).

Though Kimmitt discloses that multiplexer 108 may be used to select a final CRC output from one of the remainder registers (102a-102d), such selection is performed after the 32 bit data segments have been processed by each and every one of the CRC modules (100a-100d) and corresponding results have been stored within the remainder registers. Therefore, Kimmitt's selection of a particular remainder register does not, and cannot be used, to provide anticipatory teaching for the presently claimed steps of determining which CRC module to use for processing a current segment of data, and after such determination, processing the current segment of data using only the CRC module deemed appropriate for that data segment.

For at least the reasons set forth above, Kimmitt fails to anticipate all limitations of independent claim 1. Therefore, claim 1 and claims dependent therefrom are asserted to be patentably distinct over the cited art. Accordingly, removal of this rejection is respectfully requested.

Section 103 Rejections

Claim 2 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Kimmitt in view of U.S. Patent No. 5,050,165 to Yoshioka et al. (hereinafter "Yoshioka"). To establish a case of *prima facie* obviousness of a claimed invention, all of the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (C.C.P.A 1974); MPEP 2143.03. Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed.Cir. 1988); *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992); MPEP 2143.01. The cited art does not teach or suggest each and every limitation of the currently pending claims, some distinctive limitations of which are set forth in more detail below.

Yoshioka cannot be combined with Kimmitt to provide teaching or suggestion for the combined limitations of present claims 1 and 2. As noted above, independent claim 1 recites limitations on a method for performing a cyclic redundancy check (CRC) calculation on a data stream, where the method includes: (i) determining which one of a plurality of CRC modules -- each configured to perform the CRC calculation on a different number of bytes of data -- should be used for processing a segment of data currently supplied to the multiple-byte CRC circuit, and (ii) after said step of determining, processing the segment of data using only the CRC module determined appropriate for the current segment of data. Dependent claim 2 places an additional limitation on claim 1 by suggesting that the method may be used in an interface circuit board.

Statements in the final Office Action suggest that while "Kimmitt substantially teaches the claimed invention described in claim 1 ... Kimmitt does not explicitly teach the specific use of an interface circuit board. Yoshioka, in an analogous art, teaches [the] use of an interface circuit board." (Final Office Action, page 11). Further statements in the final Office Action suggest that "it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kimmitt with the teachings of Yoshioka by including [the] use of an interface circuit board." As described in more detail below, Kimmitt and Yoshioka fail to teach or suggest all limitations of present claims 1 and 2 and, furthermore, cannot be combined or modified to do so.

As noted above in the § 102 arguments above, Kimmitt fails to disclose all limitations of present claim 1. In addition to explicit lack of teaching, Kimmitt fails to provide motivation for the aforementioned limitations. For example, Kimmitt fails to suggest a desirability for: (i) determining which one of a plurality of CRC modules to use for processing a current segment of data, and (ii) after said determining, processing the current segment of data using only the CRC module deemed appropriate for that data segment. The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination [or modification]: *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990); MPEP 2143.01. By failing to suggest a desirability for the above-mentioned method steps, Kimmitt provides absolutely no motivation that would enable one skilled in the art to modify the teachings of Kimmitt to include such steps.

Like Kimmitt, Yoshioka also fails to teach, suggest or provide motivation for the aforementioned method steps recited in claim 1. Therefore, even if Yoshioka were to provide teaching for incorporating a CRC circuit within an interface circuit board (as suggested in the final Office Action), the combined teachings of Kimmitt and Yoshioka would still fail to disclose the combined limitations recited in claims 1 and 2.

For at least the reasons set forth above, none of the cited art, either separately or in combination, provide motivation to teach or suggest all limitations of claim 1. Therefore, claim 1 and claims dependent therefrom (claim 2) are asserted to be patentably distinct over the cited art. Accordingly, removal of this rejection is respectfully requested.

CONCLUSION

This response constitutes a complete response to all issues raised in the final Office Action mailed May 12, 2005. In view of the remarks herein traversing the rejections, Applicants assert that pending claims 1-5 and 11-20 are in condition for allowance. If the Examiner has any questions, comments, or suggestions, the undersigned attorney earnestly requests a telephone conference.

No fees are required for filing this amendment; however, the Commissioner is authorized to charge any additional fees, which may be required, or credit any overpayment, to Daffer McDaniel, LLP Deposit Account No. 50-3268/5298-10900.

Respectfully submitted,

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